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10/587,080	07/21/2006	Hiroki Mouri	28951.1181	9532

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EXAMINER	
FISCHER, MARK L	
ART UNIT	PAPER NUMBER
2627	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,080	MOURI ET AL.	
	Examiner	Art Unit	
	MARK FISCHER	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2009 and 25 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Preliminary Amendment filed on July 21, 2006 and the correction to the Preliminary Amendment filed on February 25, 2009.

2. Claims 1, 4, 6, and 9 are original, Claims 2, 3, 5, 7, 8, and 10-13 are currently amended, and Claims 14-22 are new.

Drawings

3. Figure 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 1 recites the limitation "the signal" in line 4 as well as line 6. It should be made clear "the signal" is in reference to the "digital signal" of line 3.

5. Claim 4 is objected to because of the following informalities: Line 2, "filer" should be changed to --filter--. Appropriate correction is required.

6. Claim 5, line 3, recites the limitation "said waveform equalizer", but it is unclear which of the two waveform equalizers the claim is talking about.

7. Claim 5 and 7, line 1, "Claim 1" should be changed to --Claim 1 wherein--.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 1-3, 8, 10-13, 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereinafter AAPA) in view of Tomimoto (JP 2000-243034).

Regarding claim 1, AAPA discloses (Fig. 5) a signal processing apparatus for processing a signal using a PRML (Partial Response Maximum Likelihood) method, comprising: an A/D converter (104) for converting an analog signal into a digital signal; a first waveform equalizer (106) for amplifying a specific band of the signal to optimize data of a clock extraction system, said equalizer being connected to the A/D converter; a second waveform equalizer (108) for subjecting the specific band of the signal to amplification as well as waveform equalization, thereby to optimize data of a data processing system; a timing recovery logic circuit (111) for extracting a reproduction clock, said logic circuit being connected to the first waveform equalizer; and a decoder for decoding data (109), said decoder being connected to the second waveform equalizer. AAPA does not explicitly disclose that the equalizer is connected to the A/D converter. However, Tomimoto discloses (Fig. 1) the connection of an equalizer (i.e. FIR filter 3) to an A/D converter (1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA with Tomimoto with the motivation to stabilize the reading of a signal and prevent interference between the filter 108 of AAPA and the PLL circuit (106, 107, 111, 112, 113) of AAPA.

Regarding claim 2, AAPA discloses a signal processing apparatus (Fig. 5) comprising: a variable gain amplifier (102) for automatically adjusting a signal read from a recording medium so that the signal has a desired amplitude; a filter circuit (103) for removing a signal in a specific band, said filter circuit being connected to the variable gain amplifier; an A/D converter (104) for converting an analog signal into a digital signal, said converter being connected to the filter circuit; an automatic gain controller (105) being connected to the A/D converter; a waveform equalizer (106) for performing waveform equalization, said equalizer being connected to the A/D

converter; a control circuit (107) for performing baseline control for the output of the waveform equalizer and the output of the A/D converter (the output of the A/D converter 104 is present in the output of DEQ 106) on the basis of the output of the waveform equalizer; an adaptive transversal filter (108) for amplifying a signal in a specific band as well as performing waveform equalization for a reproduction signal, the A/D converter being baseline-controlled (output of 107 is fed back to 104); a detection circuit (110) for performing error detection and correction using a LMS (Least Mean Square) algorithm, said detection circuit being connected to the adaptive transversal filter; a decoder (109) for performing maximum likelihood decoding, said decoder being connected to the adaptive transversal filter; and a timing recovery logic circuit (111) for extracting a reproduction clock, said logic circuit being connected to the control circuit. AAPA does not explicitly disclose that the adaptive transversal filter is connected to the output of the A/D converter. However, Tomimoto discloses (Fig. 1) the connection of a FIR filter (3) to the output of an A/D converter (1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA with Tomimoto with the motivation to stabilize the reading of a signal and prevent interference between the filter 108 of AAPA and the PLL circuit (106, 107, 111, 112, 113) of AAPA.

Regarding claim 3, AAPA discloses a signal processing apparatus (Fig. 5) comprising: a variable gain amplifier (102) for automatically adjusting a signal read from a recording medium so that the signal has a desired amplitude; an A/D converter (104) for converting an analog signal into a digital signal, said converter being connected to the variable gain amplifier; an automatic gain controller (105) being connected to the A/D converter; a waveform equalizer (106) for performing waveform equalization, said equalizer being connected to the A/D converter; a

control circuit (107) for performing baseline control-for the output of the waveform equalizer and the output of the A/D converter (the output of the A/D converter 104 is present in the output of DEQ 106) on the basis of the output of the waveform equalizer; an adaptive transversal filter (108) for amplifying a signal in a specific band as well as performing waveform equalization for a reproduction signal, the A/D converter being baseline-controlled (output of 107 is fed back to 104); a detection circuit (110)for performing error detection and correction using a LMS (Least Mean Square) algorithm, said detection circuit being connected to the adaptive transversal filter; a decoder (109) for performing maximum likelihood decoding, said decoder being connected to the adaptive transversal filter; and a timing recovery logic circuit (111) for extracting a reproduction clock, said logic circuit being connected to the control circuit. AAPA does not explicitly disclose that the adaptive transversal filter is connected to the output of the A/D converter. However, Tomimoto discloses (Fig. 1) the connection of a FIR filter (3) to the output of an A/D converter (1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA with Tomimoto with the motivation to stabilize the reading of a signal and prevent interference between the filter 108 of AAPA and the PLL circuit (106, 107, 111, 112, 113) of AAPA.

Regarding claim 8, AAPA discloses that the decoder is a decoding circuit using a Viterbi algorithm (see Fig. 5, element 109).

Regarding claim 10, AAPA discloses that the recording medium is an optical disc medium (Specification, Page 1, line 11).

Regarding claim 11, AAPA discloses that the recording medium is a magnetic disc medium (Specification, Page 1, lines 11-12).

Regarding claim 12, AAPA discloses that the recording medium is a semiconductor memory (Specification, Page 1, lines 12-13).

Regarding claim 13, see the rejection of claim 2 in which AAPA in view of Tomimoto discloses that data optimization for the signal in a time axis direction and data optimization for the signal in an amplitude direction are carried out using different waveform equalizers, respectively (i.e. Tomimoto suggests connecting FIR 108 of AAPA directly to the output of A/D 104, and with this configuration, DEQ 106 will carry out optimization in a time axis direction while FIR 108 will carry out optimization in an amplitude direction), and baseline control is carried out during equalization by the waveform equalizers (as seen in Fig. 5, element 107). The motivation for combination is the same as that found in the rejection of claim 2.

Regarding claim 18, see the rejection of claim 8.

Regarding claim 19, see the rejection of claim 8.

Regarding claim 20, see the rejection of claim 10.

Regarding claim 21, see the rejection of claim 11.

Regarding claim 22, see the rejection of claim 12.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Tomimoto further in view of Jones (U.S. Pat. No. 6,310,909 B1).

Regarding claim 4, AAPA discloses that the filter circuit (103) is a low-pass filter, but does not explicitly disclose that it is constituted by an order equal to or lower than third order. However, Jones discloses the use of a 3rd order LPF with a converter (Col. 6, lines 12-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

combine the teachings of AAPA in view of Tomimoto with Jones with the motivation to remove undesirable high frequency components.

13. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Tomimoto further in view of Miyashita et al. (U.S. Pub. No. 2003/0169665 A1, hereinafter Miyashita).

Regarding claim 5, AAPA in view of Tomimoto does not explicitly disclose that the waveform equalizer comprises a filter having a variable tap coefficient value, and an amplification degree thereof can be set freely and minutely. However, Miyashita discloses (Fig. 2) a waveform equalizer (11) comprises a filter having a variable tap coefficient value (as seen in Fig. 2), and an amplification degree thereof can be set freely and minutely (coefficients amplify) (paragraph [0068]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA in view of Tomimoto with Miyashita with the motivation to have a changeable filter that can adapt for better performance.

Regarding claim 6, AAPA in view of Tomimoto does not explicitly disclose that the first waveform equalizer and the second waveform equalizer are constituted by adaptive transversal filters which subject an input signal to filter processing in accordance with an equalization coefficient. However, Miyashita discloses (Fig. 2) a waveform equalizer (11) constituted by adaptive transversal filters which subject an input signal to filter processing in accordance with an equalization coefficient (as seen in Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA in view of

Tomimoto with Miyashita with the motivation to use changeable filters that can adapt for better performance.

14. Claims 7, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Tomimoto further in view of Bang et al. (U.S. Pub. No. 2005/0030660 A1, hereinafter Bang).

Regarding claim 7, AAPA does not explicitly disclose that vertical resolution of the A/D converter is 7 bits or lower. However, Bang discloses the use of an A/D converter with a 6 bit resolution (¶ [0030]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA in view of Tomimoto with Bang with the motivation to set a resolution for the A/D converter that is well-known in the art to be a reasonable value for a signal processing system using a Viterbi decoder.

Regarding claim 16, see the rejection of claim 7.

Regarding claim 17, see the rejection of claim 7.

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Tomimoto further in view of Muramatsu (U.S. Pat. No. 6,381,203 B1).

Regarding claim 9, AAPA in view of Tomimoto does not explicitly disclose an adjustment circuit for calculating a jitter value on the basis of an output of the waveform equalizer, which output is corrected by the baseline control circuit, and automatically adjusting the degree of amplification of the waveform equalizer on the basis of the calculated jitter value. However, Muramatsu discloses(Fig. 1) an adjustment circuit (70) for calculating a jitter value on

the basis of an output of the waveform equalizer (jitter detection 68 takes input from waveform equalizer 66), which output is corrected by the baseline control circuit (80), and automatically adjusting the degree of amplification of the waveform equalizer on the basis of the calculated jitter value (Col. 7, lines 1-33).

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Imanaka et al. (U.S. Pat. No. 6,580,770 B2)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK FISCHER whose telephone number is (571) 270-3549. The examiner can normally be reached on Monday-Friday from 9:00AM to 6:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Nguyen can be reached on (571) 272-7579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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4/10/2009
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